

# Large Area Imaging of Integrated Circuits Using Hard X-Ray Ptychography

Jeffrey Klug, Junjing Deng, Yi Jiang, Curt Preissner,  
Zichao Wendy Di, Tekin Bicer, Stefan M. Wild, and Stefan Vogt  
Argonne National Laboratory  
Argonne, Illinois 60439  
Email: jklug@anl.gov

Richard Sandberg and Steven Honig  
Los Alamos National Laboratory  
Los Alamos, New Mexico 87545

**Abstract**— Robust and scalable techniques for nondestructive imaging of nanometer size features in integrated circuits are of great importance for the verification and validation of current and future microelectronics devices. While electron-based microscopies provide superior spatial resolution for thin samples, destructive delayering approaches are required to image micrometer-thick structures. In contrast, hard X-ray based microscopies can allow the imaging of intact chips without destructive sample preparation. Ptychography is a coherence-based X-ray imaging technique that employs computational image reconstruction based on iterative phase retrieval to image extended objects with high spatial resolution. Currently, ptychographic imaging with  $<10$  nanometer 2D spatial resolution is routinely demonstrated over square-micrometer-scale fields of view. However, extending ptychography to millimeter and centimeter-scale imaging of samples in 3D presents nontrivial challenges in instrument design, image reconstruction, and data handling. Efficient imaging of large specimens places stringent requirements for motion trajectory errors and laser interferometry, which must be addressed through instrument hardware and control. Advanced strategies for scalable ptychography algorithms, fast tomographic reconstruction, high-performance computing, and data management will be critical. In this context, we present results of recent integrated circuit imaging experiments conducted using the Velociprobe microscope at Argonne's Advanced Photon Source. Both the current state-of-the-art and the path forward will be discussed.

**Keywords**— *ptychography; x-ray; microscopy;*

## I. INTRODUCTION

Recent work has highlighted the promise of advanced X-ray microscopy-based approaches for nondestructive imaging of nanoscale features in integrated circuit devices [1,2]. Ptychography is a coherent diffractive imaging technique capable of providing high spatial resolution of extended objects [3]. In contrast to traditional X-ray-based microscopies, such as scanning X-ray transmission microscopy, ptychography employs computational image reconstruction based on iterative-phase retrieval to achieve spatial resolution that is not limited by the X-ray beam size. Currently, ptychographic imaging with  $<10$  nanometer 2D spatial resolution is routinely demonstrated over square-micrometer-scale fields of view. Conventional tomographic reconstruction can produce 3D images by using multiple ptychographic image projections. Imaging entire devices will necessitate extending ptychography to millimeter- and centimeter-scale imaging of samples in 3D. Such scaling

presents nontrivial challenges in instrument design, image reconstruction, and data handling.

## II. THE VELOCIPROBE MICROSCOPE

The Velociprobe is a next-generation X-ray microscope built to make efficient use of the dramatic increase in coherent flux from the forthcoming Advanced Photon Source Upgrade (APS-U) [4]. Fast ptychographic imaging with high spatial resolution is achieved using novel hardware/stage designs, new positioner control designs, and new data acquisition strategies, including the use of high bandwidth interferometric measurements.

### A. Instrument Overview

The Velociprobe instrument at APS beamline 2-ID-D was designed and built to optimize stability during high-speed optics scanning for ptychography and scanning-probe measurements with an emphasis on 2D imaging. The use of novel granite, air-bearing-supported stages provides high stability during imaging. Fast, on-the-fly scanning [5] of both axes is implemented by scanning the low-mass zone plate across a small area at high speed. This is achieved by an optimized control algorithm providing large tracking bandwidth and good positioning resolution using National Instruments FPGA-based control hardware. With the current instrument, a ptychographic fly-scan of a  $4\text{ }\mu\text{m}$  by  $4\text{ }\mu\text{m}$  area with diffraction patterns captured every  $50\text{ nm}$  in both X and Y axes ( $\sim 6400$  exposures in total) can be completed in as little as 2 seconds at a speed of  $0.16\text{ mm/s}$ .

### B. Sample Stack Upgrade

High-speed, on-the-fly scanning along both zone plate axes is possible over an approximately  $9\text{ }\mu\text{m}$  by  $9\text{ }\mu\text{m}$  area. To image larger areas, the sample stages can be stepped for tile scans. However, the stepwise translation between tiles adds an overhead cost that effectively limits the scanfield to  $\sim 1\text{ mm}^2$ . Efficient imaging of larger specimens should incorporate on-the-fly scanning of one or more sample stages. This places stringent requirements for motion trajectory errors and laser interferometry which the current hardware and stages do not satisfy. Accordingly, an upgraded sample stack for the Velociprobe has been designed to accommodate large scanfields (up to  $1\text{ cm}^2$ ) without compromising the stability or performance of the original instrument.

The upgraded Velociprobe will combine a 3-axis,  $400\text{ }\mu\text{m}$  range piezo scanner (Piezosystem Jena, Tritor 400 SG) with two high-performance, linear motor, air bearing-guided linear stages

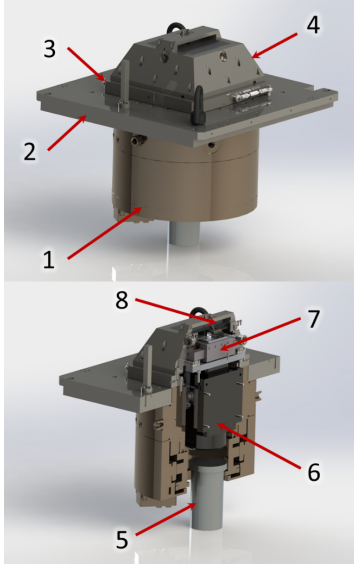


Fig. 1. CAD model of the upgraded Velociprobe sample stack, both whole and a cutaway. The components are 1) air-bearing spindle, 2) spindle mount (and sample coarse X), 3) sample stack mount, 4) metrology frame, 5) slip ring, 6) air-bearing vertical stage, 7) air-bearing horizontal stage, and 8) interferometer target and sample. Parts 2, 3, and 4 are all made of Invar.

(Physik Instrumente PIglide models A-131 and A-141) for smooth sample scanning. In addition, the existing rotation stage will be replaced with a high precision air bearing stage to minimize runout and wobble (Professional Instruments Company 10R-606 with  $<0.1 \mu\text{m}$  wobble) and thereby improve 3D tomographic reconstructions. A CAD model of the upgraded Velociprobe sample stack is shown in Fig. 1.

### III. INTEGRATED CIRCUIT IMAGING

Using the current Velociprobe we implemented tile-scanning ptychography on an integrated circuit with 16 nm technology. In the measurements, a monochromatic X-ray beam at 8.8 keV was spectrally filtered using a Si  $\langle 111 \rangle$  double-crystal-monochromator and focused by a Fresnel zone plate with an outer zone width of 50 nm. The focusing X-ray spot was 60 nm; the chip sample was placed downstream of the focus point with a beam size of about 100 nm. In each tile of the scan, the chip was imaged with an on-the-fly raster-scan trajectory with a step size of about 50 nm; the detector (Eiger 500K) acquisition rate was set to 250 frames/sec. A single tile covered  $6 \mu\text{m}$  by  $6 \mu\text{m}$ , and a total of 676 (26 by 26) tiles were acquired in about 12 hours. The raw data size of diffraction patterns was 18.5 TB. Figure 2 shows the ptychographic image, which covers a  $60 \mu\text{m}$  by  $60 \mu\text{m}$  chip area after stitching reconstructions from 100 tiles. The inset is a zoomed area taken from the red box, which covers one tile area and clearly shows the projected circuitry layers with a spatial resolution of about 12 nm.

### IV. CONCLUSION AND OUTLOOK

We have demonstrated high-resolution ptychographic imaging of an integrated circuit using our early-stage ptychographic instrument—the Velociprobe. A hardware upgrade to the instrument is currently underway to extend such

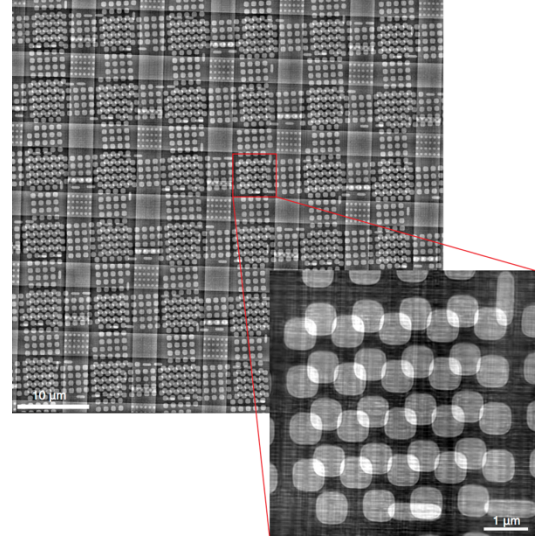


Fig. 2. Tile-scanning ptychography of an integrated circuit. The image covers 10 by 10 tiles ( $6 \mu\text{m}$  by  $6 \mu\text{m}$  per tile) which were scanned in fly-scan mode using a 8.8 keV X-ray beam. The inset is the zoomed region from the red box which shows the stacked circuit layers of this chip. The resolution unit (or pixel size) of the ptychographic image is 7 nm, the spatial resolution was estimated by line-cut profile method, which is about 12 nm.

imaging measurements from  $\mu\text{m}$ - to mm-scale fields of view. With significantly greater scan sizes, image reconstruction will present an increasing computational challenge. In the above  $60 \mu\text{m}$  by  $60 \mu\text{m}$  area chip imaging example, the raw 2D data size is about 18.5 TB. About two weeks of data reconstruction were required to produce the ptychographic image in Fig. 2 using a workstation with four Nvidia GTX 1080 Ti GPUs. As the image dimensions scale up (e.g., a few mm) and many tiled projections are acquired for 3D ptychography, the data size will be expected to increase quickly, bringing difficulties for computation. Table 1 estimates the ptychographic scan time, data size, and reconstruction time (ePIE algorithm) of 3D chip images with different fields of view. With a full detector frame rate (3 kHz at 12-bit for Eiger) and other reasonable scan parameters, the total scan time (including 20% overhead) remains feasible as the chip area increases from  $200 \mu\text{m} \times 200 \mu\text{m}$  to  $1000 \mu\text{m} \times 1000 \mu\text{m}$ . However, in the reconstruction, even with our state-of-art reconstruction software—a GPU based ePIE phase retrieval code [6], and with 200 GTX 1080 Ti GPUs, the reconstruction speed is still five times slower than the data acquisition. To tackle this computation challenge, high performance computing on a large-scale supercomputer will be utilized with high-efficiency algorithms and optimized reconstruction work flow. With algorithmic 3D developments [7] and computing developments, we expect to improve both resolution and imaged area.

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TABLE I. Estimations of scan time, data size, and reconstruction time for 3D ptychographic imaging of integrated circuits with different fields of view. Assuming that targeted resolution is 20 nm and the reconstruction code is able to decompose 10 probe modes, then a feasible step size for an on-the-fly scan will be 200 nm. The total scan time is calculated with a detector acquisition rate of 3 kHz and 20% overhead consideration. In the reconstruction, a GPU phase retrieval code based on ePIE algorithm is used with an assumption that 100 iteration arrives in convergence.

Experiment	Chip Area ( $\mu\text{m}^2$ )	200 $\times$ 200 $\mu\text{m}$	500 $\times$ 500 $\mu\text{m}$	1000 $\times$ 1000 $\mu\text{m}$
	Target Resolution (nm)	20	20	20
	Step size ( $\mu\text{m}$ ) (10 probe modes)	0.2	0.2	0.2
	Number of scan points/projection	1000000	6250000	25000000
	Diffraction pattern (pixels)	512	512	512
	Bits per pixel	32	32	32
	Data size/projection (Bytes)	1.05E+12	6.55E+12	2.62E+13
	Projections	100	100	100
	Raw data size (TB)	95.4	596.0	2384.2
	Total exposure time (days, 3 kHz)	0.4	2.4	9.6
	Total scan time (plus 20% overhead)	0.5	2.9	11.6
Computation	Number of probe modes used	10	10	10
	time/diffraction (s)/100 ePIE iterations	0.20	0.20	0.20
	Total time using one GPU (days)	231.5	1446.8	5787.0
	The number of GPUs	200	200	200
	Parallel scaling efficiency	0.5	0.5	0.5
	Reconstruction time (days)	2.3	14.5	57.9